REMARKS

Claims 1-125 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 31-39, 41, 45-49, 51-59, 61, 65-69, 71-79, 81, 85-88, 90-96, 101-107, 111-115, and 117-122 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pollanen et al. (U.S. Pat. No. 6,289,205). This rejection is respectfully traversed.

With respect to claim 31, Pollanen fails to show, teach, or suggest a voltage detector in communication with a power amplifier of a transmitter for detecting an output voltage of the power amplifier and a current detector in communication with the power amplifier for detecting an output current of the power amplifier, wherein at least one of the output voltage and the output current of the power amplifier is at least one of an output voltage and an output current of an antenna of the transmitter.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. *Scripps Clinic & Res. Found. V. Genentech, Inc.*, 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices, Inc.*, 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Pollanen fails to disclose the limitation that at least one of the output voltage and the output current of

the power amplifier is at least one of an output voltage and an output current of an antenna of the transmitter.

Exemplary embodiments of the present invention shown in FIGS. 1 and 2 illustrate a power amplifier 105 connected to an output load 108 such as an antenna. In particular, FIG. 2 shows that the power amplifier 105 is connected to the antenna at an output connection 205. In other words, an output voltage Vac and an output current Iac of the power amplifier 105 correspond to voltage and/or current of the load 108. Consequently, the power detector 120 receives a voltage signal and a current signal that are (i.e. are equivalent to) the actual voltage and/or current of the antenna (i.e. the true voltage and current output of the transmitter). The power controller 130 adjusts the power amplifier 105 accordingly.

As best understood by Applicants, FIG. 9 of Pollanen fails to disclose this structure. For example, the Examiner alleges that an amplifier included in the transmitter element 3 corresponds to the power amplifier of Applicants' claim 1. Applicants respectfully submit that output voltage and current of an alleged amplifier in the transmitter element 3 is not the output voltage and current of an antenna of the transmitter. For example, Pollanen includes a transistor T1. The transistor T1 communicates with an antenna 8. The transistor T1 amplifies an output of the transmitter element 3. In other words, at best, the output voltage and/or current of the transistor T1, (as opposed to the transmitter element 3), corresponds to the output voltage and/or current of the antenna 8. The output voltage and/or input of the alleged power amplifier in the transmitter element, which the Examiner relies on to teach the

power amplifier of claim 31, is not the output voltage and current of an antenna of the transmitter.

In view of the foregoing, Pollanen fails to show, teach, or suggest that at least one of the output voltage and the output current of the power amplifier is at least one of an output voltage and an output current of an antenna of the transmitter. Applicants respectfully submit that claim 31 should be allowable for at least the above reaons. Claims 32-125 should be allowable for at least similar reasons.

REJECTION UNDER 35 U.S.C. § 103

Claims 1-8, 10-23, 42-44, 62-64, 82-84, 97-99, 108-110, and 123-125 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Pollanen et al.(U.S. Pat. No. 6,289,205) in view of McGirr et al. (U.S. Pat. No. 5,129,098). This rejection is respectfully traversed.

With respect to claim 1, Pollanen, either singly or in combination with McGirr, fails to show, teach, or suggest a voltage scaling ratio controller for controlling a voltage scaling ratio of the voltage scaler to maintain the voltage signal within a predetermined voltage range based on a plurality of stored target output power levels and corresponding voltage scaling ratios.

An exemplary embodiment shown in FIG. 1 of the present invention illustrates a voltage detector 110 that includes a voltage scaler 135 and a ratio controller 150. The ratio controller 150 "can be comprised of any type of processor and computer memory. The voltage scaling ratio controller 150 can set the voltage scaling ratio of the voltage scaler 135 based upon a predetermined target output power of the power amplifier 105.

For example, the system 100 can have a plurality of associated target output power levels...each target output power level can be associated with a different voltage scaling ratio." (Paragraph [0070]). In other words, the voltage scaling ratio controller 150 controls the voltage scaling ratio to maintain the voltage signal within a predetermined voltage range based on a plurality of stored target output power levels and corresponding voltage scaling ratios.

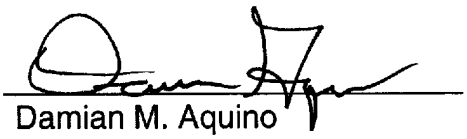
In contrast, the Examiner alleges that FIG. 9 of Pollanen discloses a voltage scaling ratio controller A1. Applicants respectfully note that element A1 is a comparator. The comparator A1 receives inputs from transistor T1. As such, the comparator A1 does not control a voltage scaling ratio based on a plurality of stored target output power levels and corresponding voltage scaling ratios as claim 1 recites. Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claim 16, as well as its dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: November 6, 2006

By: 
Damian M. Aquino
Reg. No. 54,964

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

MDW/mp